## IN THE CLAIMS

Please amend claims 1-5, 6 and 26, as set forth below.

Please add new claim 36, as set forth below.

The text of all pending claims, along with their current status, is set forth below:

1. (Currently Amended) A ~~vertical tunneling transistor~~ device, comprising:

a memory element disposed on a substrate, and

an access device coupled to the memory element, the access device comprising:

a channel disposed on ~~a~~ the substrate;

a quantum dot disposed so that the channel is between the quantum dot and the substrate, wherein the quantum dot is comprised of at least one of tungsten, tin, platinum, or rhodium;

a gate disposed so that the quantum dot is between the gate and the channel; and

wherein an axis through the channel, the quantum dot, and the gate is substantially perpendicular to an upper surface of the substrate.

2. (Currently Amended) The device ~~vertical tunneling transistor~~ set forth in claim 1, comprising a source disposed on the substrate adjacent to the channel.

3. (Currently Amended) The device ~~vertical tunneling transistor~~ set forth in claim 1, comprising a drain disposed on the substrate adjacent to the channel.

4. (Currently Amended) The device ~~vertical tunneling transistor~~ set forth in claim 1, comprising a tunneling barrier disposed between the channel and the quantum dot, wherein the tunneling barrier comprises at least one of tantalum carbide or halfnium oxide.

5. (Currently Amended) The device ~~vertical tunneling transistor~~ set forth in claim 1, comprising an insulative layer disposed between the quantum dot and the gate.

6. (Currently Amended) An integrated circuit device, comprising:

a substrate; and

a memory array that includes a plurality of memory cells disposed on the substrate, each of the plurality of memory cells comprising a memory element and an access transistor, the access transistor comprising:

a channel disposed on the substrate;

a self-aligned quantum dot disposed so that the channel is between the quantum dot and the substrate, wherein the quantum dot is comprised of at least one of tungsten, tin, platinum, or rhodium;

a gate disposed so that the quantum dot is between the gate and the channel; and

wherein an axis through the channel, the quantum dot, and the gate is substantially perpendicular to an upper surface of the substrate.

7. (Original) The integrated circuit device set forth in claim 6, comprising a source disposed on the substrate adjacent to the channel.

8. (Original) The integrated circuit device set forth in claim 6, comprising a drain disposed on the substrate adjacent to the channel.

9. (Previously Presented) The integrated circuit device set forth in claim 6, comprising a tunneling barrier disposed between the channel and the quantum dot, wherein the tunneling barrier comprises at least one of tantalum carbide or halfnium oxide.

10. (Original) The integrated circuit device set forth in claim 6, comprising an insulative layer disposed between the quantum dot and the gate.

11-25. (Cancelled)

26. (Currently Amended) A vertical tunneling transistor, the vertical tunneling transistor produced by the process of:

disposing a channel on a substrate;

disposing a dielectric layer on the substrate;

providing an aperture with a sidewall in the dielectric layer;

disposing a spacer adjacent the sidewall in the aperture that reduces a dimension of the aperture that is substantially parallel to the substrate to a sub-photolithographic size;

disposing a quantum dot within the aperture so that an axis through the channel and the quantum dot is substantially perpendicular to the substrate, wherein the quantum dot is comprised of at least one of tungsten, tin, platinum, or rhodium; and

providing a gate so that an axis through the channel, the quantum dot and the gate is substantially perpendicular to the substrate.

27. (Original) The vertical tunneling transistor set forth in claim 26, wherein the process comprises employing atomic layer deposition to provide the channel.

28. (Original) The vertical tunneling transistor set forth in claim 26, wherein the process comprises employing atomic layer deposition to provide the quantum dot.

29. (Original) The vertical tunneling transistor set forth in claim 26, wherein the process comprises employing atomic layer deposition to provide the gate.

30. (Original) The vertical tunneling transistor set forth in claim 26, wherein the process comprises disposing a source adjacent to the channel.

31. (Original) The vertical tunneling transistor set forth in claim 26, wherein the process comprises disposing a drain adjacent to the channel.

32. (Previously Presented) The vertical tunneling transistor set forth in claim 26, wherein the process comprises providing a tunneling barrier, wherein the tunneling barrier comprises at least one of tantalum carbide or halfnium oxide.

33. (Original) The vertical tunneling transistor set forth in claim 26, wherein the process comprises employing atomic layer deposition to provide a tunneling barrier.

34. (Original) The vertical tunneling transistor set forth in claim 26, wherein the process comprises providing an insulative layer.

35. (Original) The vertical tunneling transistor set forth in claim 26, wherein the process comprises employing atomic layer deposition to provide an insulative layer.

36. (New) The vertical tunneling transistor set forth in claim 26, wherein the process comprises coupling the vertical tunneling transistor to a memory element.